SPECIFICATION AMENDMENTS

Please amend the Specification as shown below:

[0041] FIGURE 3 illustrates operation of the processor 20 compared to operation of a conventional synchronous implementation. Whereas the conventional implementation operates continuously and relatively uniformly on incoming chips, the processor 20 does the required amount of processing at the fastest clock rate available in a serial fashion. This speed enables the processor 20 to finish its processing before the time needed for the next buffer to fill and require servicing (i.e., a Symbol Group Duration). As shown in FIGURE 3, prior to an end of a first Symbol Group Duration, the [[The]] processor 20 can be shut down (i.e., the clock is gated off) through a remainder of and until the completion of the first Symbol Group Duration, and the processor 20 is enabled at the beginning of a next Symbol Group Duration that occurs consecutively with the end of the first Symbol Group Duration. As also shown in FIGURE 3 by the width of block sections, the given amount of processing may vary from Symbol Group to Symbol Group.